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# **JEDEC ENGINEERING BULLETIN**

**No. 5-A**

**METHODS OF MEASUREMENT FOR SEMICONDUCTOR**

**LOGIC GATING MICROCIRCUITS**

**JEDEC**  
Solid State Products Engineering Council

METHODS OF MEASUREMENT FOR SEMICONDUCTOR  
LOGIC GATING MICROCIRCUITS

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## FOREWORD

The test methods and other material included herewith are recommended for use in the rating of semiconductor logic gating microcircuits which use the binary states to represent and process logic information. Both static and dynamic measurements are covered. These methods of measurement are equally applicable to monolithic, multichip, film or hybrid device construction, whether of silicon, germanium, or other semiconductor material, whether incorporating bipolar or MOS or both types of transistor technology.

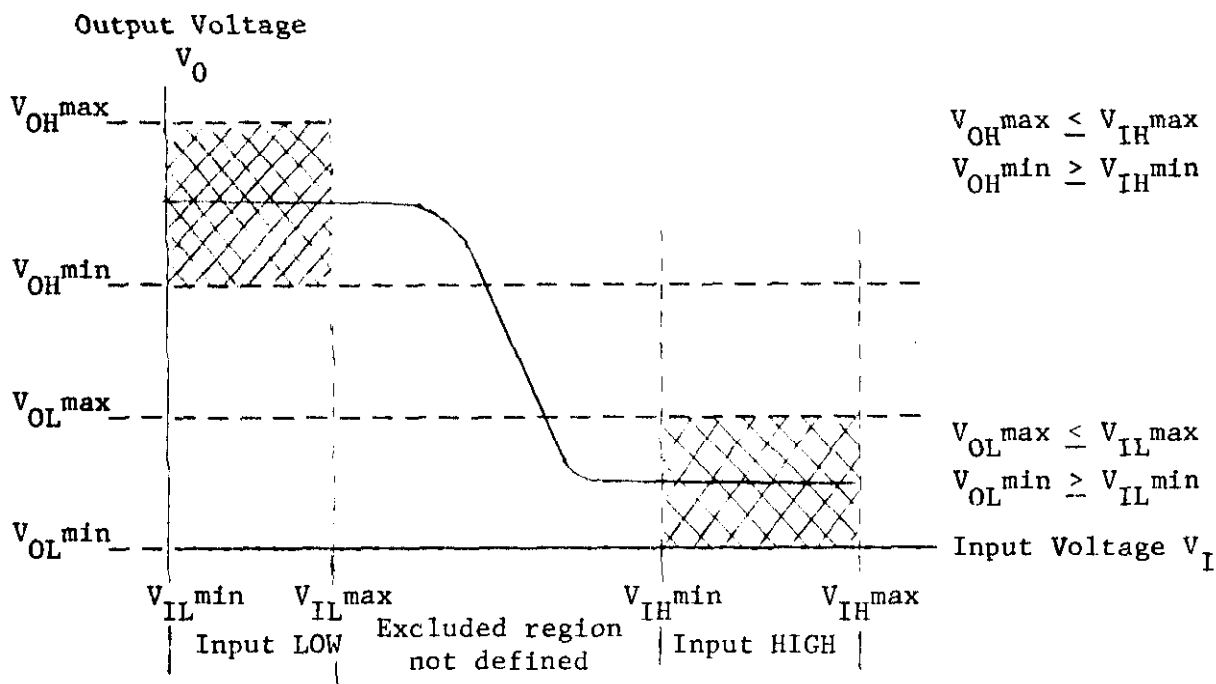
The purpose of this bulletin is twofold. It is to describe recommended tests and test methods, as noted above. It is also intended to assist and instruct those who complete and use the EIA Registration Data format for semiconductor logic gating microcircuits, MED-32-1C.

This document has been prepared by the MED-32 Committee on Active Digital Circuits and has been approved for publication by the EIA Microelectronics Engineering Panel.

## GENERAL BACKGROUND

For the circuit configurations of semiconductor logic gating microcircuits which use binary states to represent the digital information, a logical relationship exists between input and output. The logical conditions can be identified by the electrical parameters measured on the input and output to describe the binary states. Voltages or currents may be used to describe the states, but voltage is used most commonly.

The diagram of Figure 1 shows the state of the output of a gating circuit as a function of the input, using voltages to represent the states. There are certain limits that can be applied to each of the states to identify the acceptable operating regions for a particular design. Thus, on Figure 1, which is for an inverting logic gate, the output voltage must be within the cross-hatched areas for the defined voltages that appear at the input.  $V_{IHmin}$ ,  $V_{ILmax}$ ,  $V_{IHmax}$ , and  $V_{ILmin}$  are the boundaries of these regions. Since the logic gating circuits must couple to each other, the same values apply to input and output. The cross-hatched regions represent the regions of DC stability for the input and output voltages under worst case conditions for any logic gating circuit in a digital system made up of such gates.



OUTPUT VS INPUT VOLTAGE FOR AN INVERTING LOGIC GATING MICROCIRCUIT

Figure 1

$V_{ILmax}$  is the maximum allowed input LOW level in a logic system;  $V_{IHmin}$  is the minimum allowed input HIGH level in a logic system. For any  $V_I$  value less than  $V_{ILmax}$  or greater than  $V_{IHmin}$ , but less than  $V_{IHmax}$  the output voltage must be in the cross-hatched area.  $V_{IHmax}$  is chosen to be at least as large as the maximum HIGH state output can be. It will generally be the supply voltage unless the output has an active rather than a resistive pull-up.  $V_{ILmin}$  is chosen to be at least as small as a minimum LOW state output can be. It generally is zero and is shown so in Figure 1 and used so in the following test condition.

## MINIMUM DC CHARACTERISTICS FOR INTERCHANGEABILITY

In setting the registration format for semiconductor logic gating microcircuits, it was found that a universal set of "black-box" specifications could not be settled on without getting very cumbersome. Therefore, the format has been divided according to the type of circuit configuration of the logic gating circuit. A certain minimum amount of information is required to assure interchangeability. The format contains what is considered the minimum information necessary to describe a logic gate.

The inverting logic function is assumed in most of the format and in the commentary and curves which follow. Transposition of the worst-case conditions for non-inverting logic should be made as appropriate.

### DEFINITIONS

HIGH and LOW Levels The HIGH (H) level is that level which is the most positive of the two logic levels whereas the LOW (L) level is that level which is the most negative of the two logic levels.

Positive and Negative Logic Positive logic identifies the logic ONE with the HIGH level and logic ZERO with the LOW level. Negative logic identifies the logic ONE with the LOW level and the logic ZERO with the HIGH level.

Positive Current Conventional current flow into a microcircuit terminal is defined as positive.

Maximum Limit The highest-magnitude limit of a range of some quantity. For logic levels only, the most positive (least negative) limit.

Minimum Limit The lowest-magnitude limit of a range of some quantity. For logic levels only, the least positive (most negative) limit.

Logic Gating In the titles of this bulletin and the registration data format, the term "logic gating" is used. This is meant to cover all combinatorial logic functions and to exclude sequential logic functions. The latter, because they have memory, are covered by the bistable bulletin and registration data or some extension of it. Thus all interconnections of logic gates inside the registered microcircuit are within the applicability of this bulletin on logic gating microcircuits, provided that no inverting gates are cross-coupled (the output of gate A drives an inverting input of gate B and the output of gate B drives an inverting input of gate A) or the equivalent or obtain logic memory in any other manner.

For additional definitions, see also EIA format MED-32-1C, "Registration Data, Semiconductor Logic Gating Microcircuit," Appendix I.

Microelectronics Engineering Bulletin 1A, "Recommended Microelectronic Terms and Definitions."

## COMMENTARY ON THE REGISTRATION DATA FORMAT

Numbering herein is identical to that used in the MED-32-1C format for semiconductor logic gating microcircuits.

### 1.0 GENERAL DESCRIPTIONS

1.1 Type of Device specifies semiconductor material.

1.2 Type of Logic Function and Polarity describes the number of separate gates within the device and the logic function provided (NANA, AND, NOR, OR, COMBINATIONAL, etc.) and specifies whether positive or negative logic is meant.

1.3 Number of Inputs identifies all inputs to the device. This includes the number of inputs to each section of the device as well as expanding nodes for increasing fan-in or performing other logic functions externally.

1.4 Number and Type of Outputs describe the number and electrical type (open collector, emitter follower, etc.) of external outputs from each gate. It should be stated if logic can or should not be performed by connecting outputs together.

2.0 LOGIC DESCRIPTION The device must be completely described with a logic diagram, logic equations, and a truth table relating inputs to outputs.

2.1 The Logic Diagram represents the circuit function symbolically. Each terminal (inputs and outputs) must be identified with letters for reference to the logic equation and truth table. The preferred logic symbols are those defined in "Graphic Symbols for Logic Diagrams," IEEE Publication No. 91/ANS Y32.14.

2.2 The Logic Equation relates each output to the inputs. This equation must be consistent with the type and polarity of logic function described in Section 1.2 and the terminal identification in Section 2.1.

2.3 The Truth Table shows the relations between the HIGH (H) or LOW (L) logic levels of the inputs and outputs. The "HIGH/LOW" designation should be used in the truth table to avoid any confusion between positive or negative logic notation. Generally every column corresponds to the level of an input or output and every line corresponds to a combination of the input level and the resulting output level or levels. Whenever the level of an input has no influence it should be indicated by the symbol "X."

3.0 MECHANICAL DATA No commentary beyond notes incorporated in the registration data format is necessary.

4.0 MAXIMUM RATINGS A maximum rating is a limiting value of voltage, current or temperature which is to be exceeded only at the risk of permanently altering the characteristics of the microcircuit. A combination of maximum ratings cannot normally be permitted simultaneously.

#### 4.1 Temperature

4.1.1 Storage Temperature Range defines the range of environment in which a microcircuit may be stored with no electrical connections to the device.

4.1.2 Temperature Range under Bias defines the temperature range in which the microcircuit may be operated without risk of permanent change. The intent of this paragraph is to state the allowable maximum temperature in a system under some fault condition of cooling with supply voltages still applied. No guarantee of correct logic operation is intended. Both the temperature range and the bias conditions must be specified. Bias should represent that set of expected extreme continuous operating conditions of supply voltages, input drive, and output loading which result in worst-case power consumption. If the operating frequency has any significant effect on power consumption, a normal operating frequency shall be specified.

4.2 Terminal Voltage and/or Current Terminal Voltage and/or Current defines the maximum voltage and/or current that may be safely applied to each terminal of the microcircuit without risk of permanently altering any of its characteristics. Note that these ratings must be guaranteed over a specified temperature range and that this temperature range must include the temperature extremes specified for electrical characteristics under paragraph 5.1.2.2 but not necessarily those specified under paragraph 4.1.2. Each of these maximum values is defined independently of all others. For example, if a maximum power supply voltage is specified at 10 V and a maximum output current is specified to be 50 mA, the 10 V and 50 mA conditions cannot necessarily be applied simultaneously. In addition, if the maximum values specified apply only for certain conditions on other terminals, then these relevant conditions must also be specified. When maximum ratings are specified for both voltage and current at the same terminal, these maximum values are not defined independent of one another. For instance, if a maximum output voltage is specified at 8 V and a maximum current is specified to be 30mA for the same output, neither rating may be exceeded in attempting to apply the other.

#### 5.0 ELECTRICAL CHARACTERISTICS

5.1 Operating Conditions The notes in the registration data format are sufficient for use and understanding. No additional commentary is needed.

#### 5.2 Static Characteristics

A. For registration of static characteristics, three alternate sequences of tests are provided. These sequences relate to the three main circuit types in use:

5.2.1 DCTL, RTL and RCTL

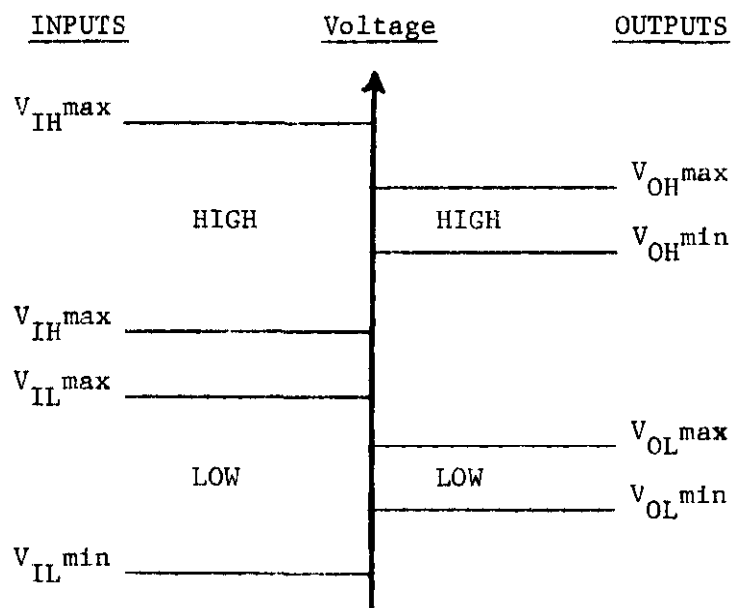
5.2.2 DTL and TTL

5.2.3 ECL



One of these sequences, where applicable to the type of circuit configuration used, should be chosen. For multiple duplicate gates, these tests apply for each gate. For more complex combinations of gates, these tests should serve as guiding rules in specifying the circuits. Conditions on all terminals must be specified for each test.

- B. The first two items in each sequence (5.2.X.1 and 5.2.X.2) are not tests. They are definitions of input logic voltage levels. This is the starting point for the registration of all electrical parameters. They are, by nature, definitions of the maximum and minimum LOW (L) and HIGH (H) voltage levels which will be accepted and recognized by the registered device. These do not appear as parameters in the format. The validity of the definitions is proven by using them as conditions and verifying that they do result in proper logical operation according to the truth tables of paragraph 2.2. They are used for both Static and Dynamic characteristics. Generally, the output levels of a logic gate are intended to be compatible with its input requirements. The logic gate output is intended to drive other logic gates like itself or other logic elements in the same family having compatible input requirements. Therefore, a relationship generally exists as depicted in Figure 2.
- C. In the descriptions and comments which follow, for each of the three sequences of tests, the same paragraph numbering is used as that given in the registration data format. Description of many of the tests is clarified by reference to Figures showing certain electrical characteristics. The test points are located by "X's" and are keyed to the text by circled numbers. The numbers are the least significant (right-most) part of the decimal number of the respective test.



Relationship between Input and Output HIGH and LOW Levels

FIGURE 2

5.2.1 Static Characteristics of DCTL-RTL Type Digital Circuitry This section will serve to illustrate the application of the logic gating format to an RTL type gate. This can best be illustrated with the aid of a transfer characteristic curve which is labeled with both the EIA standard terminology and the corresponding terminology most commonly employed in current RTL literature; see Figure 3.

With the aid of this curve the terms can be interpreted as follows:

5.2.1.1 A:  $V_{IL}^{min}$  - The minimum voltage that can be applied at the input of an RTL gate. In principle this may be zero volts. In practice, this would normally be output of a heavily saturated gate.

B:  $V_{IL}^{max}$  - The maximum low level voltage that can be applied to the input of an RTL gate and maintain that gate in the logical high state ( $V_{OH} \geq V_{OHmin}$ ). This is commonly referred to as  $V_{OFF}$  in RTL literature.

5.2.1.2 A:  $V_{IH}^{min}$  - The minimum high level voltage that can be applied to an RTL gate to guarantee that the gate output will maintain the logical low condition ( $V_{OL} \leq V_{OLmax}$ ). This is commonly referred to a  $V_{ON}$  in RTL literature. The purpose of this measurement is to establish the guaranteed value of  $I_{available}$  for fanout purposes. This current is normally specified at the  $V_{IH}$  required to drive the next gate load. In RTL circuitry, this measurement is more meaningful at that value of  $V_{IH}$  that guarantees "hard" saturation ( $V_{IN}$  in RTL literature).  $V_{IHmax}$  is only achieved at a fanout of one which defeats the purpose of the measurement.

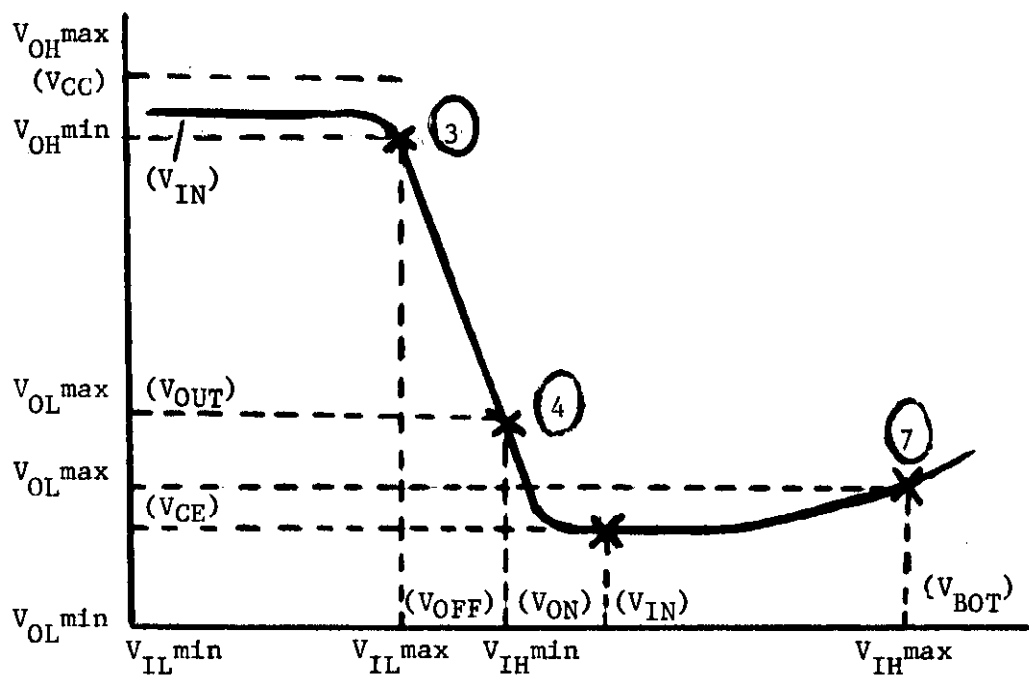
B:  $V_{IH}^{max}$  - The maximum high level voltage that will be applied to an RTL gate under normal operation. Commonly referred to as  $V_{BOT}$  in current RTL literature.

5.2.1.3  $V_{OH}^{min}$  - The minimum value of output voltage realizable with a known current, under conditions of maximum reverse bias current in the output gate transistor. In RTL literature, this is usually expressed in terms of the voltage for which a guaranteed  $I_0$  ( $I_{available}$ ) is obtainable.

5.2.1.4  $V_{OL}^{max}$  - The maximum value of output voltage realizable with the gate in the logical low condition, sinking a specified load current  $I_0$ , with a minimum high level drive  $V_{IHmin}$  ( $V_{ON}$ ) applied. Commonly referred to as  $V_{OUT}$  in RTL literature.  $I_0$  represents the  $I_{CER}$  reverse bias current of the driven gates.

5.2.1.5  $I_{IHmax}$  - The maximum input current which will flow when all other inputs are simultaneously biased high with at least the minimum high threshold voltage. This current is referred to as  $I_{IN}$  in the literature. At the other inputs, most RTL specifications use a voltage greater than  $V_{IHmin}$ ; normally  $V_{BOT}$ .

- 5.2.1.6  $I_{OH}^{max}$  - The maximum current that will flow with the worst-case input "off" voltage applied and an output voltage greater than  $V_{OHmin}$  at the gate output. The closest equivalent in most RTL literature is an  $I_L$  test which measures the current into the  $V_{CC}$  lead. The  $I_{OH}$  measurement is performed on some gate expander elements in the literature.
- 5.2.1.7 A:  $V_{OL}^{max}$  - The purpose of this test is to define the condition of "hard" saturation. The idea is to establish the the output voltage level under maximum input drive conditions to aid in determining the relative system noise margin available in the design.
- B:  $V_{OL}^{max}$  - The purpose is generally to ensure that the output voltage remains below  $V_{OL}^{max}$  even with all inputs simultaneously high at maximum  $V_{IH}$ . If appreciable emitter resistance were present, the test might be a worst case.
- 5.2.1.8  $I_{OH}^{max}$  - No comment, similar to test 5.2.1.3.
- 5.2.1.9  $I_{IH}^{max}$  - This measurement is equivalent to 5.2.1.5 except that it permits measuring directly the input current at a voltage greater than the input threshold voltage. Normally, in RTL this current is measured at  $V_{IN}$  and is referred to as  $I_{IN}$ . See the discussion on  $I_{IN}$  under paragraph 5.2.1.5.
- 5.2.1.10  $I_O^{max}$  - The test is designed to measure the total current drain from the  $V_{CC}$  supply with the input and outputs normally grounded. In RTL it is a direct measure of the output resistor.
- 5.2.1.11  $V_O^{max}$  - This measurement is intended exclusively for use with the gate extender type elements. Normally, the  $I_O$  current is matched to what would be expected if an internal output resistor were attached.



VOLTAGE TRANSFER CHARACTERISTIC FOR DCTL, RTL, AND RCTL (5.2.1)

Figure 3

5.2.2 Static Characteristics for DTL and TTL Type Logic Gating Circuitry  
 This section will serve to illustrate the application of the logic gating format to the registration of circuits such as DTL and TTL. Understanding of the definitions (5.2.2.1 and 5.2.2.2) and tests (5.2.2.3 ff) may be facilitated by reference to the electrical characteristic curves given in Figures 4, 5, 6, and 7. The test points are shown in these figures by "X's" and are keyed to the tests by circled numbers. These numbers are the least significant part of the decimal number of the respective tests.

5.2.2.1 A:  $V_{ILmin}$  - The minimum LOW level voltage applied to the gate input.

B:  $V_{ILmax}$  - The maximum LOW level voltage that can be applied at the gate input and still maintain the gate output at a logic HIGH level.

5.2.2.2 A:  $V_{IHmin}$  - The minimum HIGH level voltage that can be applied at the gate input and still maintain the gate output at a logic LOW level.

B:  $V_{IHmax}$  - The maximum HIGH level voltage applied to the gate input.

5.2.2.3  $V_{OLmax}$  - The maximum LOW level output voltage sinking a specified load current  $I_0$  while  $V_I = V_{IHmin}$  is applied to all inputs simultaneously.

5.2.2.4  $I_{ILmax}$  - The maximum LOW level input current flowing into the gate when  $V_I \leq V_{ILmax}$  is applied to each input sequentially, other inputs  $V_I = V_{IHmax}$ .

5.2.2.5 A:  $I_{IHmax}$  - The maximum current with  $V_I \geq V_{IHmin}$  applied sequentially to each input with other inputs at  $V_{ILmin}$  and measured at  $I_0 = 0$ .

B:  $I_{IHmax}$  - The maximum current with  $V_I \geq V_{IHmin}$  applied sequentially to each input with other inputs open or to  $V_{IHmin}$  and measured at  $I_0 = 0$ .

5.2.2.6 HIGH Level Output with  $V_I = V_{ILmax}$  applied to each input sequentially, other inputs to  $V_I \geq V_{IHmin}$ .

A:  $I_{OHmax}$  - This is a measure of the output high current into the output terminal, for outputs having no current source (pull-up).

B:  $V_{OHmin}$  - This is a measure of the minimum HIGH level output voltage when the output is sourcing a specified current.

5.2.2.7  $I_{0max}$  and/or  $I_{0min}$  - The output current available from the device. This represents the short circuit current flowing while the inputs have  $V_I = V_{ILmin}$  applied to them simultaneously.

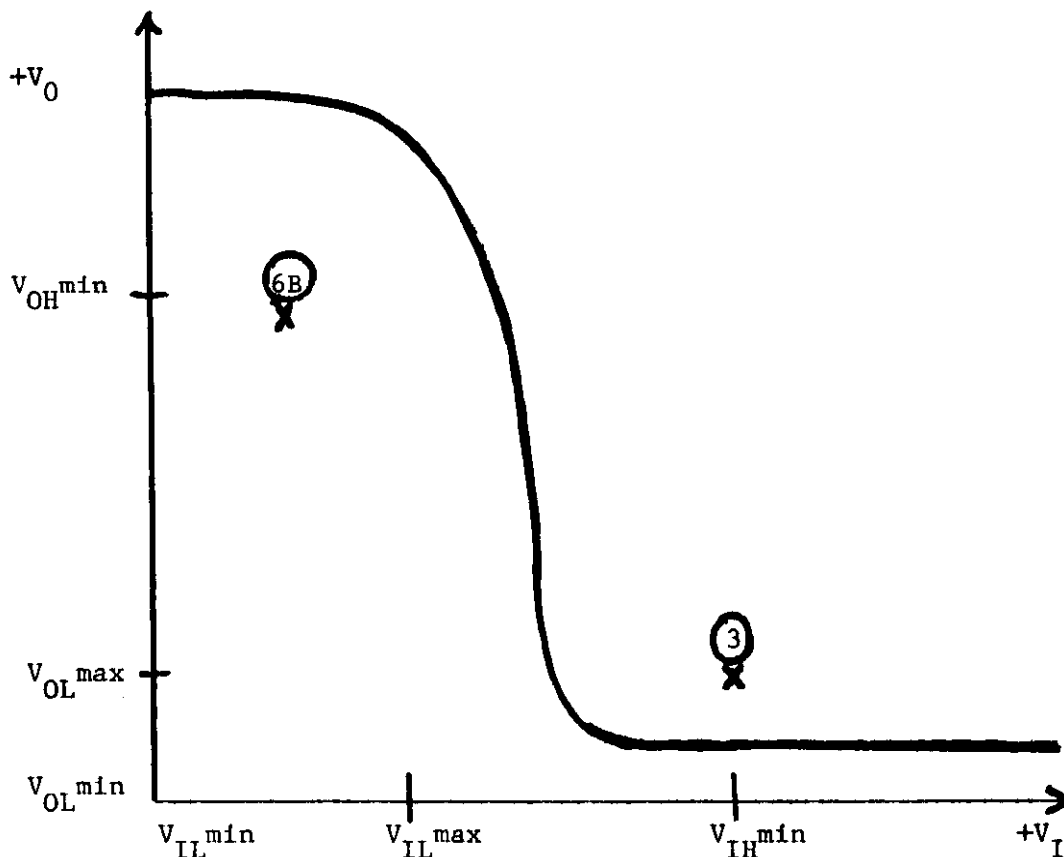
5.2.2.8  $I_{INL}^{max}$  - This is a measure of the maximum input current on the expander input node of an expandable DTL gate. This current is measured with the expander node held to a logic LOW level.

5.2.2.9 HIGH Level Output with  $V_{INL}$  applied to the expander node input, with other inputs open or to  $V_I \geq V_{IH}^{min}$ .

A:  $I_{OH}^{max}$  - This is a measure of the output HIGH current into the output terminal, for outputs having no current source (pull-up).

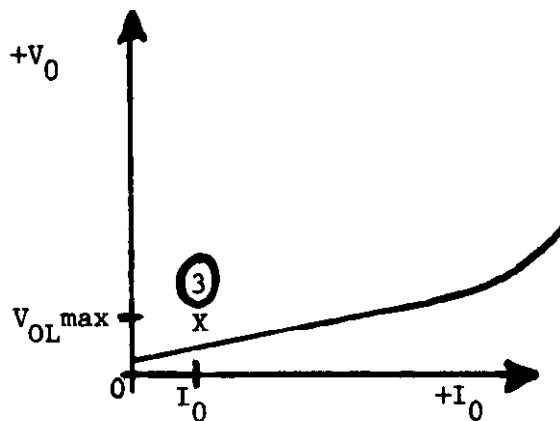
B:  $V_{OH}^{min}$  - This is a measure of the minimum HIGH level output voltage when the output is sourcing a specified current with the expander node held to a logic LOW level.

5.5.5.10  $I_R^{max}$  and/or  $I_R^{min}$  - This is a test to calculate the resistance of the output resistors when they are not internally connected to the output transistors. This current is measured with a voltage  $V_R \leq V_{IL}^{max}$  applied to the resistor terminals.



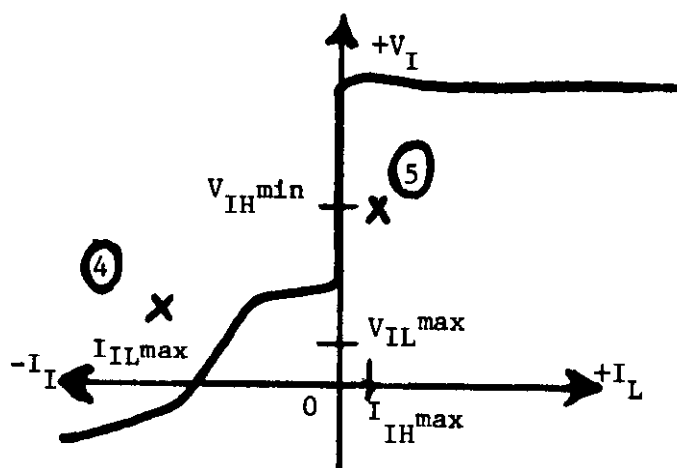
VOLTAGE TRANSFER CHARACTERISTIC FOR DTL AND TTL (5.2.2)

Figure 4



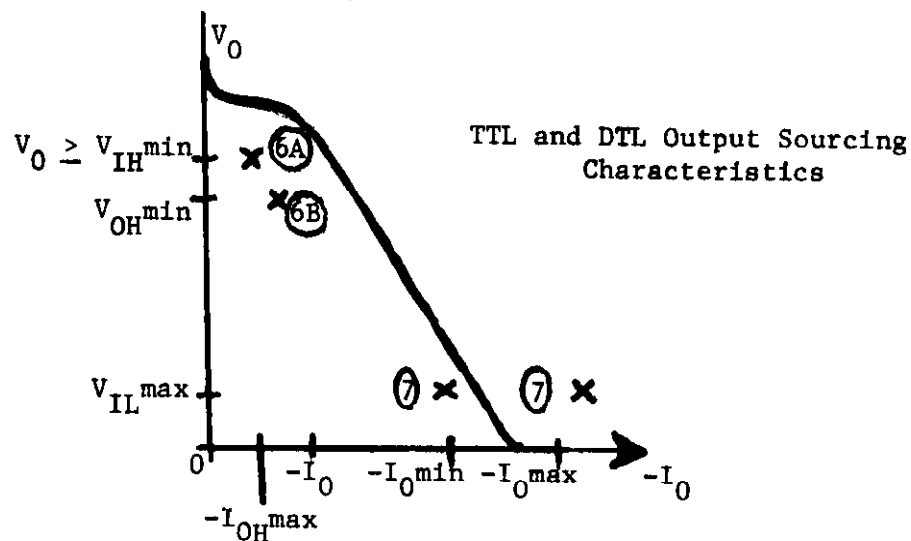
OUTPUT SINK CURRENT CHARACTERISTIC FOR DTL AND TTL (5.2.2)

Figure 5



INPUT V-I CHARACTERISTIC FOR DTL AND TTL (5.2.2)

Figure 6



OUTPUT SOURCE CURRENT CHARACTERISTIC FOR DTL AND TTL (5.2.2)

Figure 7

5.2.3 Static Characteristics for Emitter Coupled Logic This section defines parameters which are applicable to the emitter-coupled logic (ECL) type of logic gate and which are measured at the time the ECL gate is in a stable electrical and logical state. This stable state will be the result of static input and output applied conditions. A representative ECL circuit schematic is shown in Figure 8.

Each of the following statements, except 5.2.3.5, 5.2.3.18 5.2.3.19 are referenced to points of typical characteristic curves shown in Figures 9, 10 and 11. The least significant decimal number of each statement's reference number is shown beside the representative point. The reason for the exclusion of reference points for statements 5.2.3.5, 5.2.3.18 and 5.2.3.19 will become apparent when they are explained below.

5.2.3.1 These statements are input logic voltage level definitions.  
and See 5.2.B above for comments and see Figure 2 above.

5.2.3.2

5.2.3.3 Reference Voltage - If the registered ECL gate device requires a reference voltage, it will be defined here. The registrant has the option of defining a single reference voltage (and its tolerance) for all temperatures or specifying the reference voltage (and its tolerance) at each temperature.

5.2.3.4  $I_{OHmin}$  - This is a definition of the minimum HIGH state output current level which will guarantee a minimum fan-out capability of the device.

5.2.3.5 Output Load - This definition is a requirement to ensure that the output stage is performing as an active emitter-follower when verifying the output voltage parameters in tests 5.2.3.7, 5.2.3.9, 5.2.3.10, 5.2.3.11, 5.2.3.12, 5.2.3.13, and 5.2.3.15. When the circuit has an internal load resistor, the parameter verification measurements will be performed without altering the emitter-follower current. When there is no internal load resistor, an output current must be specified for each specified test.

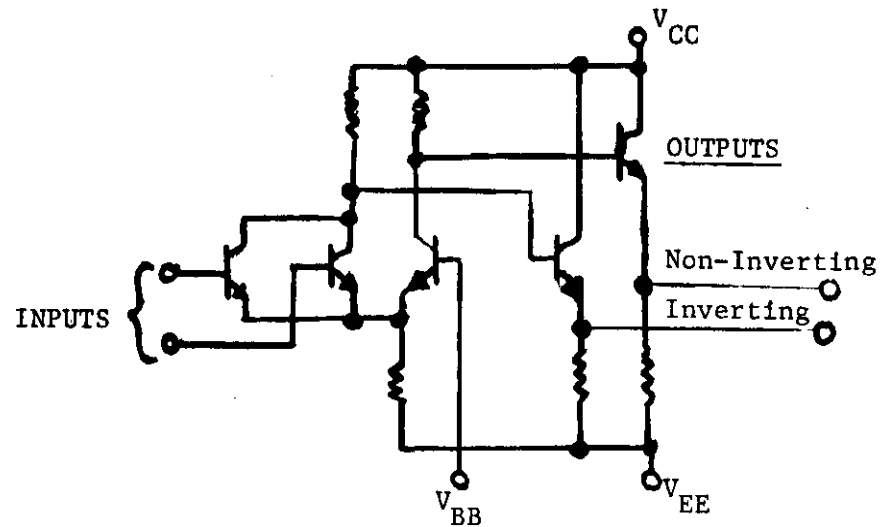
5.2.3.6  $\Delta V_{OHmax}$  - This is an optional test indicating the maximum decrease in output voltage from no load to full load which indicates the output impedances of the device. Because  $V_{OHmin}$  is measured at  $I_O = I_{OHmin}$ , this  $\Delta V$  characteristic is accounted for in 5.2.3.8 and 5.2.3.14 of the format.

NOTE: Statements 5.2.3.7 through 5.2.3.11, and 5.2.3.18 apply to the inverting outputs, while statements 5.2.3.12 through 5.2.3.15, and 5.2.3.19 apply to non-inverting outputs. The other statements apply to the general case.



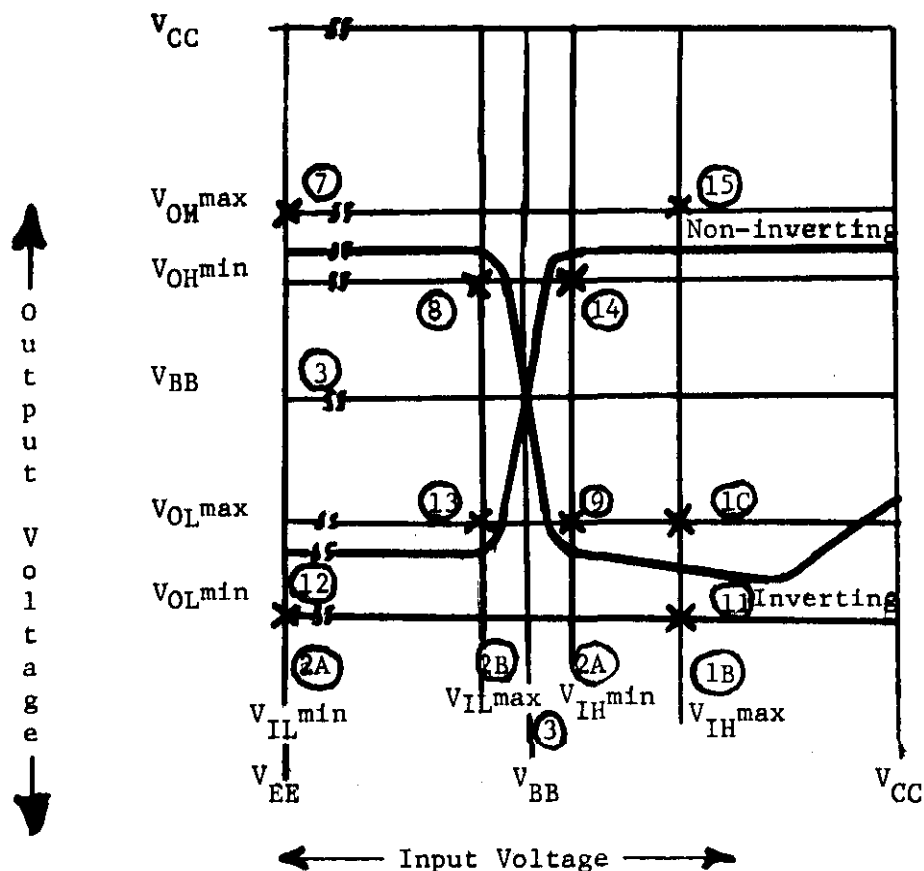
- 5.2.3.7 V<sub>OHmax</sub> - This is a required test to assure that the worst-case HIGH outputs are not greater than the worst-case HIGH inputs to the device. The object of this measurement is to verify that excessively large output voltage swings will not occur, which, when connected to a like device, could cause that device's gate input transistors to saturate at elevated temperatures.
- 5.2.3.8 V<sub>OHmin</sub> - The worst-case input levels are intended to verify that the minimum output HIGH state voltages are sufficient to represent HIGH level to the inputs of like devices.
- 5.2.3.9 V<sub>OLmax</sub> - This is a required test to assure that each input at the minimum HIGH level will cause LOW state outputs and that the output voltage levels will be less than, or equal to, the required worst-case, maximum LOW input voltages at the gate's input.
- 5.2.3.10 V<sub>OLmax</sub> - This is an optional test for the device, at maximum operating temperature, which is designed to indicate the absence of saturation.
- 5.2.3.11 V<sub>OLmin</sub> - This is a required test to assure that the gate input transistors will not saturate at elevated temperatures. Saturation would be due to an improper ratio of the input gate's collector resistor to the emitter resistor.
- 5.2.3.12 V<sub>OLmin</sub> - for OR outputs. The purpose of this test is the same as 5.2.3.11 above.
- 5.2.3.13 V<sub>OLmax</sub> - This is a required test to assure that worst-case LOW state inputs will cause the outputs to be less than, or equal to, the same worst-case input voltage level.
- 5.2.3.14 V<sub>OHmin</sub> - This is a required test to assure that worst-case HIGH state inputs will cause the outputs to have sufficient voltage to drive inputs with the same worst-case level.
- 5.2.3.15 V<sub>OHmax</sub> - The purpose of this test is to assure no saturation as described in statement 5.2.3.7.
- 5.2.3.16 I<sub>IHmax</sub> - This is a required test to determine the worst-case HIGH state input current of each input terminal of the device. This value, in conjunction with I<sub>OHmin</sub> (test 5.2.3.4), is used to determine fanout of the device.
- 5.2.3.17 I<sub>ILmax</sub> - This is a required test to determine the worst-case, input terminal leakage current of each input for the device.
- 5.2.3.18 I<sub>Qmin</sub> and/or I<sub>Qmax</sub> - for inverting outputs. The test conditions on this optional test reverse biases the output emitter follower base-emitter junction and the resultant current flow may be used to determine the value of the internal load resistors.
- 5.2.3.19 I<sub>Qmin</sub> and/or I<sub>Qmax</sub> - for non-inverting outputs. The test conditions on this optional test reverse biases the output emitter follower base-emitter junction and the resultant current flow may be used to determine the value of the internal load resistors.

A representative schematic of an ECL logic gate is shown below.



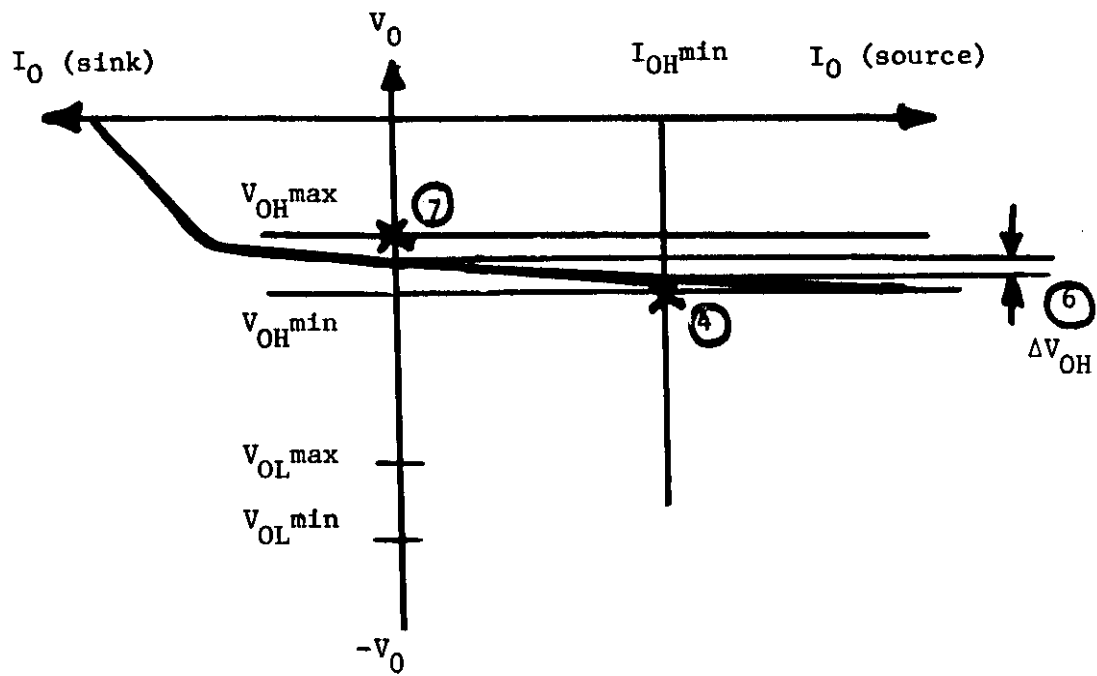
REPRESENTATIVE SCHEMATIC OF ECL GATE (5.2.3)

Figure 8



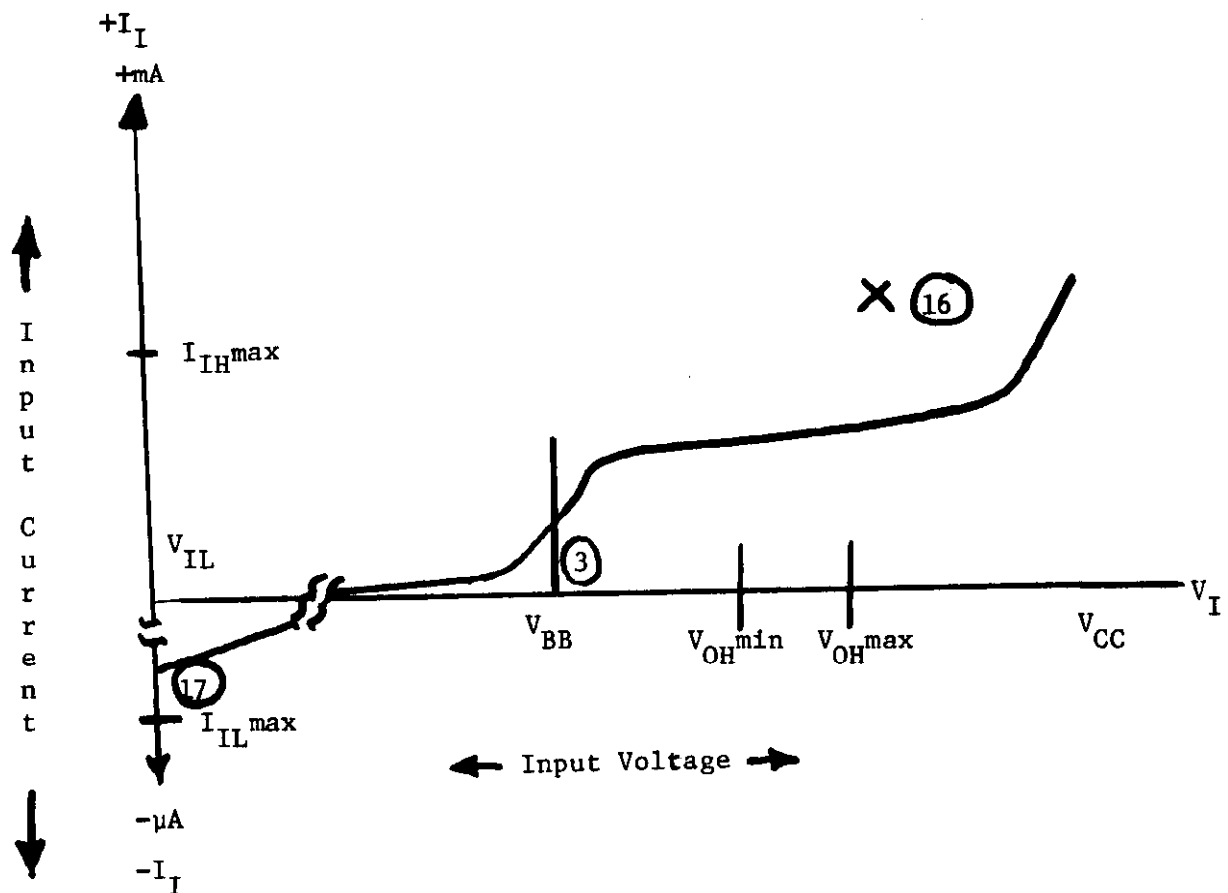
VOLTAGE TRANSFER CHARACTERISTIC FOR ECL (5.2.3) SHOWING BOTH INVERTING AND NON-INVERTING CURVES

Figure 9



OUTPUT V-I CHARACTERISTIC FOR ECL GATE (5.2.3)

Figure 10



INPUT V-I CHARACTERISTIC FOR ECL GATE (5.2.3)

Figure 11

### DYNAMIC CHARACTERISTICS - GENERAL (5.3)

In the following, standard measurement techniques are presented for the characterization of the switching times of logic gating microcircuits. The propagation delay time measurement is intended to provide information relative to the performance of the microcircuit in a typical operating system where both the driving and loading networks are either similar logic gates or an accurate simulation of these gates. The transition time measurements are intended to characterize the gate under specific loading conditions which simulate similar logic gates or different circuits of the same family such as bistable. In order to insure complete interchangeability, both propagation delay and transition time measurements are required. The principal intent is to specify unambiguous switching time measurements independent of component selection, scopes and generators, and jig building techniques.

A method of measurement for transition delay times is included to provide further dynamic characteristics although these times are not given in the registration data format. They may be estimated from the propagation delay and output transition time values.

This information is meant to clarify and elaborate on the measurements required by the logic gating registration data format. To help relate this bulletin to the format, the applicable section number of the format is shown in parentheses after most paragraph headings.

#### DEFINITIONS (5.3)

Common terms used in these measurements are defined below:

Circuit - The specific microcircuit in question or different microcircuits of the same family.

Network - Passive and/or active components (transistors and diodes only) used for input driving and output loading functions.

C.U.T. - Microcircuit under test.

V<sub>ILmin</sub> - V<sub>IHmin</sub>

V<sub>ILmax</sub> - V<sub>IHmax</sub>

See-Section 5:2, "Static Characteristics"

#### Propagation Delay Times (5.3.1)

The propagation delay times are the delays which result when a change in logic level propagates from the input of a logic gating circuit to the output of that circuit. They are defined in terms of the change in logic level at the output, as follows:

t<sub>PLH</sub> - is the propagation delay time measured with the specified output changing from the defined LOW level to the defined HIGH level with respect to the corresponding input transition.

t<sub>PHL</sub> - the propagation delay time measured with the specified output changing from the defined HIGH level to the defined LOW level with respect to the corresponding input transition.

The propagation delay times are measured as indicated in Figure 12. Note the 10% allowed on the effective switching threshold voltage:  $1/2 (V_{ILmax} + V_{IHmin})$  is an allowable range of definition. A single value within this range must be specified.

#### Output Transition Times (5.3.2)

The transition times of the waveform at the output of the logic gating circuit shall be defined in terms of the following parameters as shown in Figure 13.

t<sub>TLH</sub> - the transition time measured with the specified output changing from the defined LOW level to the defined HIGH level.

t<sub>THL</sub> - the transition time measured with the specified output changing from the defined HIGH level to the defined LOW level.

In the above definitions the transition times are measured between specified voltage levels on the output waveform. The HIGH level voltage ( $V_H$ ) must lie between  $V_{IHmin}$  and  $V_{IHmax}$  and the LOW level voltage ( $V_L$ ) must lie between  $V_{ILmin}$  and  $V_{ILmax}$ . Note that the voltage levels specified for the t<sub>TLH</sub> measurements may be different from those specified for the t<sub>THL</sub> measurement.

#### Transition Delay Times\*

The transition delay times are defined in terms of the following parameters as shown in Figure 14:

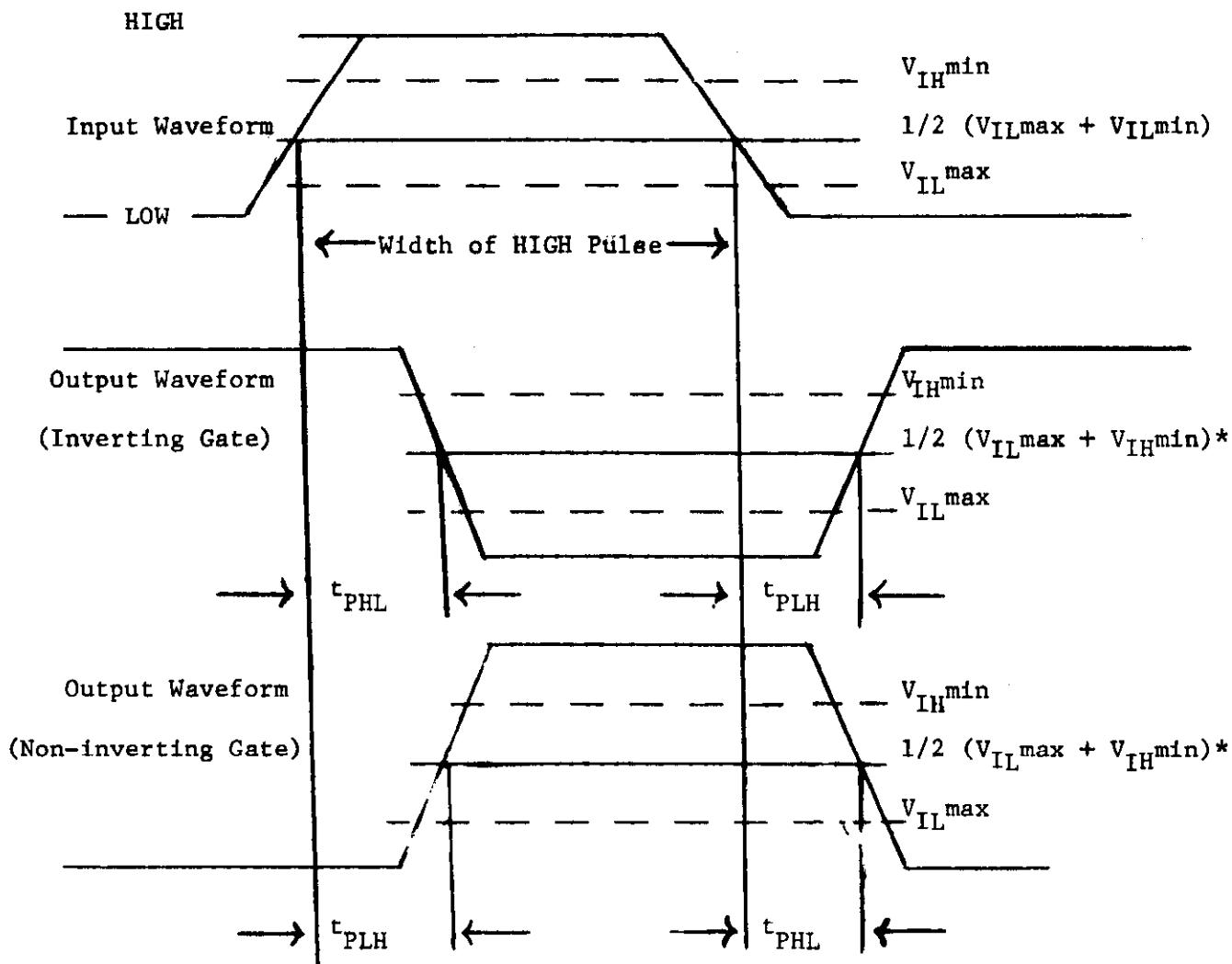
t<sub>DLH</sub> - the transition delay time measured with the specified output changing from the defined LOW level to the defined HIGH level with respect to the corresponding input transition.

t<sub>DHL</sub> - the transition delay time measured with the specified output changing from the defined HIGH level to the defined LOW level with respect to the corresponding input transition.

In the above definitions the transition delay times are measured between specified voltage levels on the input and output waveforms. The HIGH level voltage ( $V_H$ ) must lie between  $V_{IHmin}$  and  $V_{IHmax}$  and the LOW level voltage ( $V_L$ ) must lie between  $V_{ILmin}$  and  $V_{ILmax}$ . Note that the voltage level measurement points used on the input must be the same as those established on the output.

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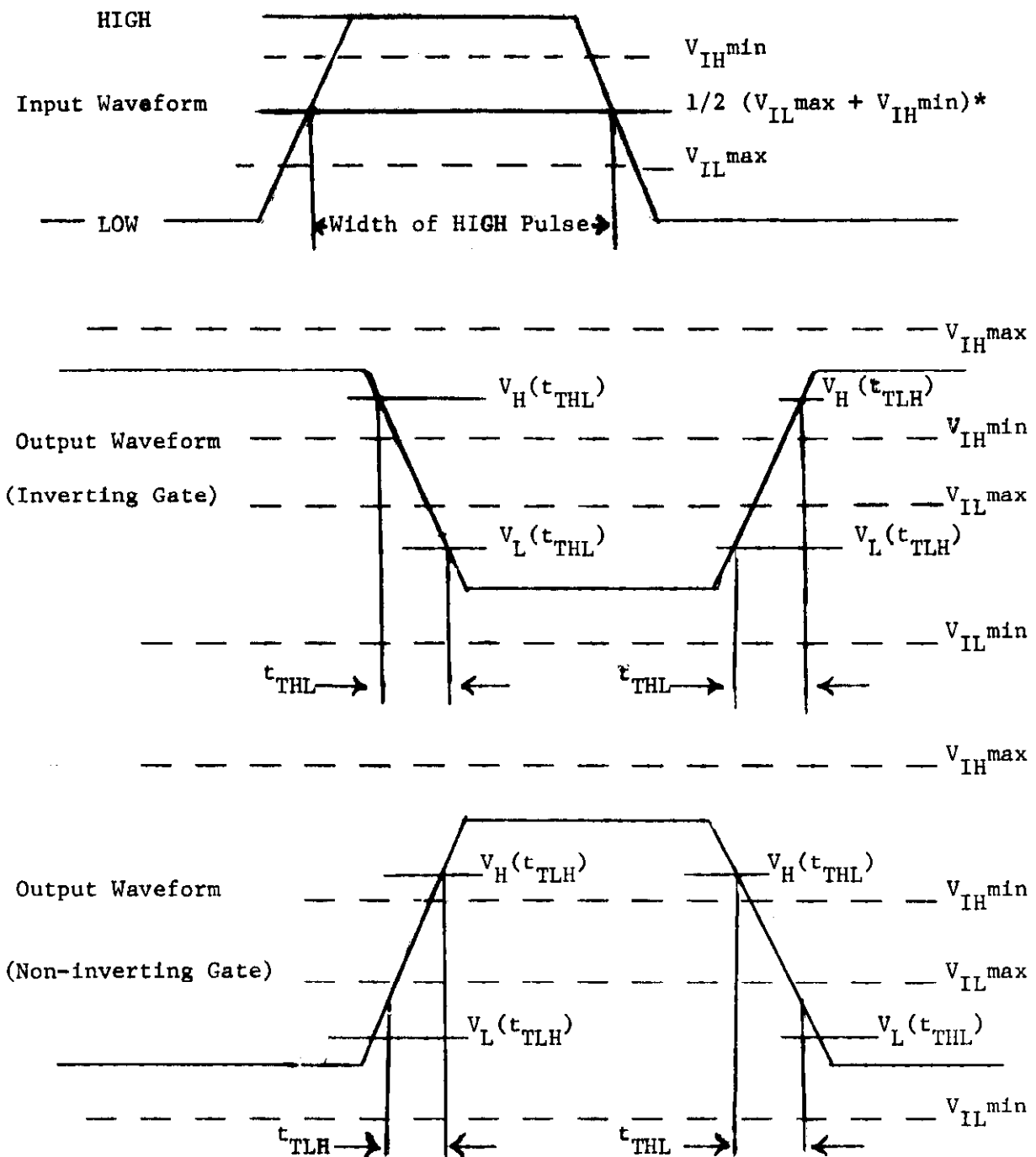
\* Not listed in format; see comment under GENERAL (5.3) above.



\* The range on the voltage level " $1/2 (V_{ILmax} + V_{IHmin})$ " is  $\pm 10\%$  of this value or  $\pm 10\%$  of " $(V_{IHmin} - V_{ILmax})$ ," whichever is greater. A single value must be specified.

#### PROPAGATION DELAY MEASUREMENTS ON WAVEFORMS

Figure 12

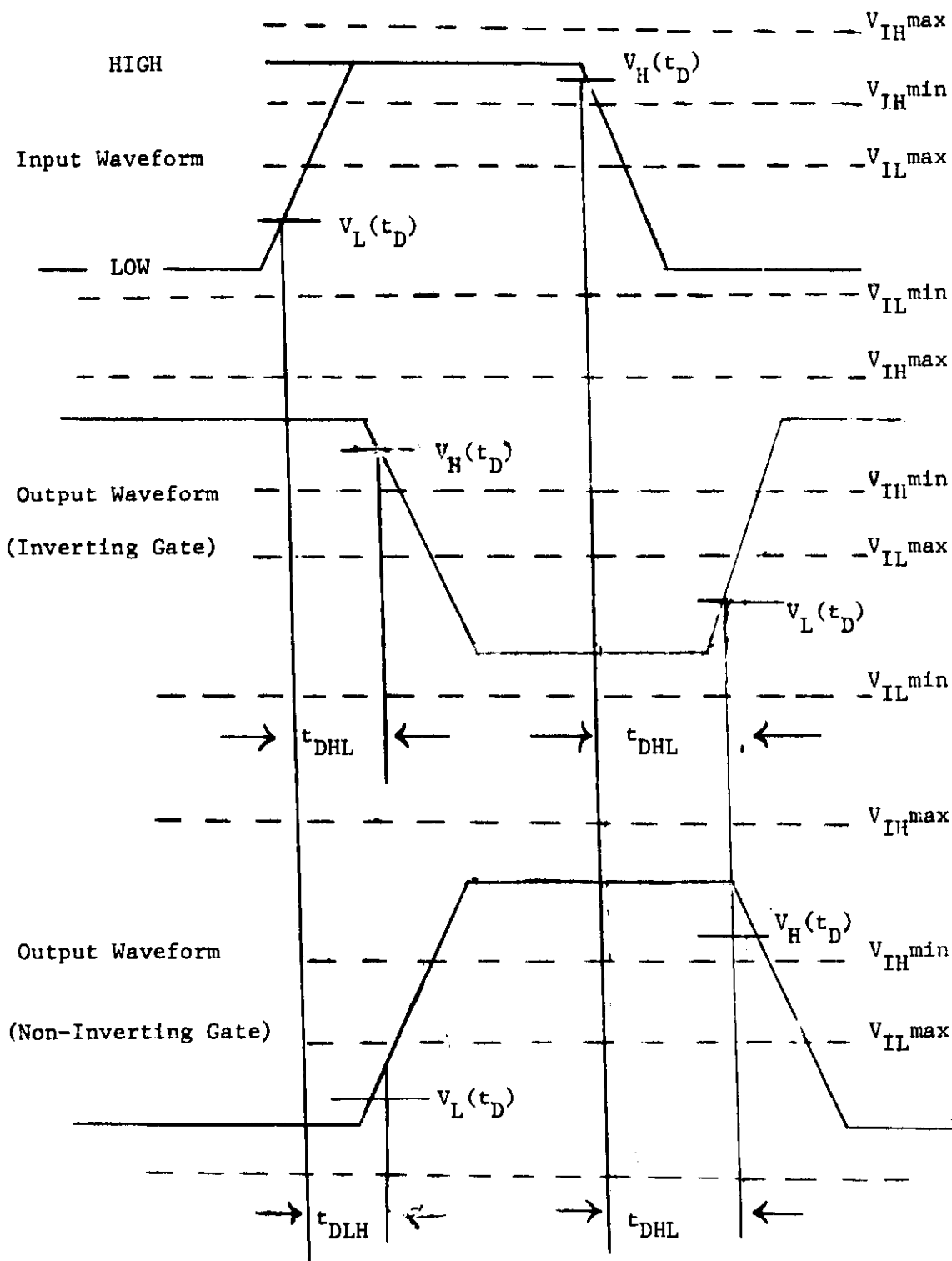


**NOTE:**  $V_{IL}^{min} \leq V_H(t_{THL}) < V_{IH}^{max}$   
 $V_{IH}^{min} \leq V_H(t_{TLH}) < V_{IH}^{max}$   
 $V_{IL}^{min} < V_L(t_{THL}) \leq V_{IL}^{max}$   
 $V_{IL}^{min} < V_L(t_{TLH}) \leq V_{IL}^{max}$

\* See \* of Figure A.

OUTPUT TRANSITION TIMES MEASURED ON WAVEFORMS

Figure 13



NOTE:  $V_{IH\min} \leq V_H(t_D) < V_{IH\max}$

$V_{IL\min} < V_L(t_D) \leq V_{IL\max}$

TRANSITION DELAY MEASUREMENT ON WAVEFORMS

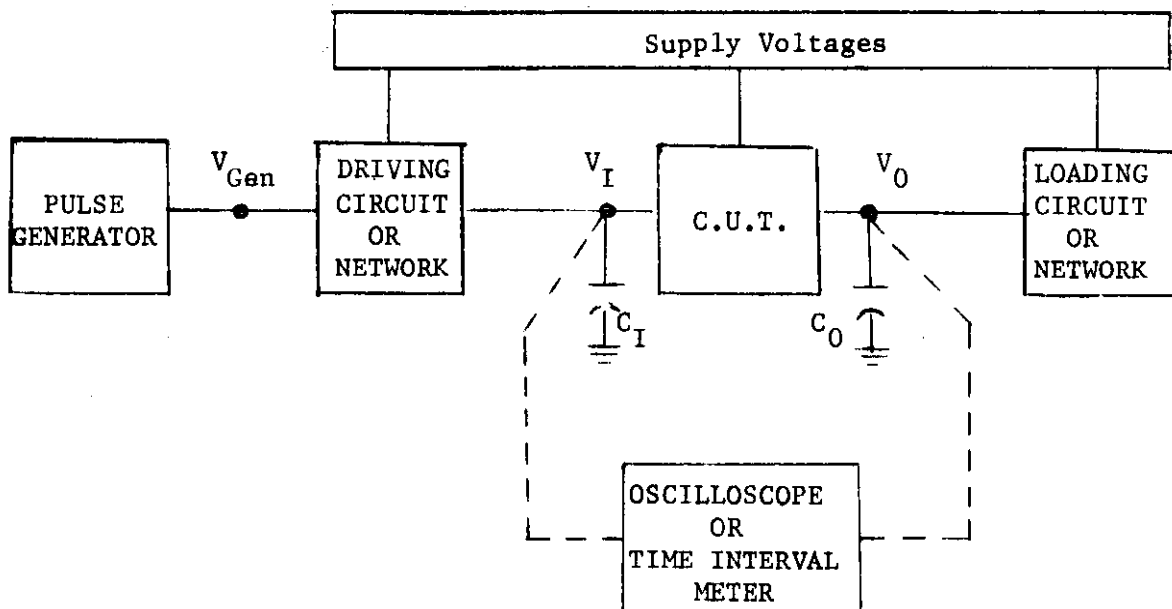
Figure 14



### TEST SETUP (5.3.1.3 & 5.3.2.3)

The dynamic characteristics shall be determined by means of measurements made with the test setup shown in the block diagram of Figure 15. Either logic gating circuits or discrete component networks may be used for driving and loading the C.U.T., according to the characteristic being measured. The specific requirements are given in the sections which follow, but, in brief, the following table summarizes the requirements:

<u>Time Measurement</u>	<u>Driving</u>	<u>Loading</u>
Propagation Delay Times	circuit or network	circuit or network
Output Transition Times	circuit or network	network
Transition Delay Times	circuit or network	network



TEST SETUP FOR DYNAMIC MEASUREMENTS

Figure 15

## CONDITIONS FOR TIME MEASUREMENTS (5.3.1.3 & 5.3.2.3)

### Supply and Bias

The DC supply and bias conditions including the bias on all unused inputs and outputs of the C.U.T. shall be specified. The bias on unused inputs and outputs of driving and/or loading circuits shall be specified where appropriate.

### Circuits

Where logic circuits are used for driving or loading the C.U.T., the circuits shall have typical characteristics representative of the family to which the C.U.T. belongs.

The logic gating circuit used for driving shall have transition time and voltage level characteristics which are typical of the C.U.T. An exception will be a logic gating (interface) circuit which is not intended to be driven by similar circuits. If additional circuits are tied to the output of the driving circuit to simulate additional loading, the number of circuits added, M, shall be specified.

The logic gating circuit(s) used for loading shall have input voltage-current and capacitive characteristics typical of the C.U.T. A similar exception to that above is appropriate. If more than one loading circuit is used to simulate greater fanout, the number, N, shall be specified.

### Networks

Networks for driving and loading shall be specified by means of a circuit diagram and component values or type numbers. The time constants and impedances of the networks should be determined primarily by the passive components used. Active components, referenced by EIA 1N or 2N type numbers or equivalent, may be used to establish driving or loading networks representative of the C.U.T. or of the use of the C.U.T., but if used they shall be sufficiently faster in response than the C.U.T. and/or sufficiently shunted by passive (linear) capacitors, so that by using any other active component of the type specified or equivalent, the time measurement reading shall not be affected within the accuracy of the measurement.

If the waveform at the output of the driving network has a critical effect on the dynamic characteristics of the C.U.T., a waveform which simulates the output of a typical microcircuit of the same type must be provided. The driving network may be simply the terminating resistor for the pulse generator, if appropriate.

The loading network used for propagation delay time measurements must simulate the input voltage-current characteristic of a typical microcircuit of the same type as the C.U.T., and must simulate the appropriate fanout. Nonlinear components such as diodes and transistors will generally be required in addition to linear, passive components in the loading network. Care should be exercised in the choice of active components to assure that the critical component parameters are controlled by the registered characteristics; as an example, a parameter which may be critical to the loading network for TTL is transistor inverse beta.

An advantage of a loading-network over use of a typical microcircuit as load is the precision of specification, resulting in a more reproducible measurement. Also, the difficulty of wiring many gates together to simulate a large fanout is avoided.

#### Driving Waveform Definitions

The following definitions shall apply both to the pulse generator waveform and to the waveform resulting from the driving network or circuit.

Pulse Width - shall be specified at the same voltage level as that used for propagation delay time.

Transition Times - shall be specified using the same voltage levels as those used for the output transition time measurements.

#### Driving Waveform Specification

The values for the pulse generator source impedance shall be specified. Values for pulse transition times (rise and fall), repetition rate, amplitude levels (both HIGH and LOW), and pulse width shall be specified for either the output waveform of the generator, or the output waveform of the network, or the waveform presented at the C.U.T. input terminal. If passive components only, or passive components and diodes only, are used in the driving network, the pulse generator waveform may be specified. If active components other than diodes are used in the driving network, then the network output waveform or the waveform at the C.U.T. input must be specified.

#### Capacitances

The capacitances at the input and output of the C.U.T., designated  $C_I$  and  $C_O$ , respectively, should include all stray capacitances associated with the mounting jigs and test fixture but should exclude parasitic capacitances presented by the C.U.T. and the driving and loading circuits, where applicable. The parasitic capacitance present in the driving and loading networks, where applicable, shall be included either in  $C_I$  and  $C_O$  or in the network descriptions, if appropriate.

#### POWER SUPPLY CURRENT DRAIN (5.4)

No commentary is needed to augment the notes in the registration data format.

ELECTRONIC INDUSTRIES ASSOCIATION  
REGISTRATION DATA  
SEMICONDUCTOR LOGIC GATING CIRCUIT

*This format is intended for the registration of semiconductor logic gating microcircuits, including Monolithic, Multichip, Film, and Hybrid Logic Gating Microcircuits, as defined in Appendix A.*

\* 1.0 GENERAL DESCRIPTION

1.1 Type of Device

This device is a germanium, silicon, etc. semiconductor logic gating microcircuit.

1.2 Type of Logic Function and Polarity

This device is a single, dual, triple, quadruple, etc., NAND, AND, NOR, OR, Combinational, etc. logic gating microcircuit for positive, negative logic.

1.3 Number of Inputs

This device has two, three, etc. logic inputs to each gate and one, two, three, etc. node terminals for expanding fan-in to each gate (or similar statement).

1.4 Number and Type of Output(s)

This device has one, two, three, etc. output(s) from each gate which is (are) described logically in Section 2. The output(s) may or may not be connected together, combined with, (or similar statement) other outputs to perform OR logic (or similar statement).

1.5 Functional Electrical Schematic

A representative functional electrical schematic is included for reference only.

\* 2.0 LOGIC DESCRIPTION

*Inverting logic is assumed for this format. If non-inverting logic is being registered, it must be so stated. The transposition of the worst-case conditions should be made as appropriate.*

2.1 Logic Diagram (See Figure \_\_)

*The logic gating microcircuit should be represented by a logic diagram (use of the symbolic shapes in "Graphic Symbols for Logic Diagrams," IEEE Publication No. 91/ANS Y32.14, latest revision is preferred).*

2.2 Logic Equation (See Figure \_\_)

*The logic gating circuit's logic equations relating inputs to outputs shall be provided.*

2.3 Truth Table (See Figure \_\_)

*A Truth Table relating the states of pertinent inputs and outputs should be provided. This need not be a complete Truth Table but must call out the important operating states.*

\* 3.0 MECHANICAL DATA

3.1 Outline

*An EIA registered outline for packages is recommended. If no applicable registered outline exists, an outline drawing must be furnished in conformance with "Registered Outlines and Descriptive Rules for Microelectronic Products and Carriers," MED Bulletin No. 13. Terminals that are omitted must be counted and the maximum remaining length of such omitted terminals must be given. Refer to EIA rules for numbering package leads.*

3.2 Terminal Designations

*Terminal assignments shall be referenced to the logic diagram called out in Section 2.1.*

<u>Terminal</u>	<u>Assignment</u>
1	_____
2	_____
3	_____
4	_____
-	_____
-	_____
-	_____
-	_____
N	_____
Case	_____
	<i>Indicate all unconnected terminals as "NC."</i>
	<i>If electrically connected to a package terminal or any portion of the circuit, it should be so indicated.</i>

3.3 Handling Precautions *Include all necessary handling precautions.*

3.4 Mounting Positions *Include any restrictions on mounting positions.*

3.5 Mounting Techniques *Include recommendations for mounting and connecting to external leads (e.g. soldering, welding, etc.). State if the case is electrically conductive or nonconductive.*

\* 4.0 MAXIMUM RATINGS (Maximum ratings are limits which should never be exceeded.)

4.1 Temperature

4.1.1 Storage Temperature Range,  $T_{stg}$  \_\_\_\_\_ °C to \_\_\_\_\_ °C

4.1.2 Temperature Range Under Bias,  $T_{A(ambient) \text{ or } T_{C(case)}}$  \_\_\_\_\_ °C to \_\_\_\_\_ °C

*With specified supply voltages and specified worst-case input-output conditions applied, the temperature either ambient or case must remain between the points specified.*

(Conditions are specified below.)

<u>Supply Voltages</u>	<u>Conditions on All Terminals</u>	
	<u>Inputs</u>	<u>Outputs</u>
$V_{CC} =$ _____ V		
$V_{EE} =$ _____ V		
$V_{BB} =$ _____ V		
$V_{other} =$ _____ V		

4.2 Terminal Voltage and/or Current

*Maximum voltage and/or current limits at any one or all terminals referenced to a common terminal shall be specified for the specified (ambient or case) temperature range.*

*The range must include the temperature extremes specified for electrical characteristics under paragraph 5.1.2.2.*

*Specify conditions on all other terminals where relevant.*

$T_{A(ambient) \text{ or } T_{C(case)}}$  \_\_\_\_\_ °C to \_\_\_\_\_ °C

<u>Terminal</u>	<u>Voltage</u>	<u>Current</u>
All supplies	_____ and/or _____	_____ and/or _____
All inputs	_____ and/or _____	_____ and/or _____
All outputs	_____ and/or _____	_____ and/or _____
Nodes	_____ and/or _____	_____ and/or _____

All voltage limits referenced to terminal number \_\_\_\_\_.

## 5.0 ELECTRICAL CHARACTERISTICS

### 5.1 Operating Conditions

#### \* 5.1.1 Nominal Supply Voltage

$V_{CC}$  \_\_\_\_\_

$V_{EE}$  \_\_\_\_\_

$V_{BB}$  \_\_\_\_\_

$V_{other}$  \_\_\_\_\_

*In each of the static and dynamic tests to be described the nominal value of all supply voltages is applied unless otherwise noted by the registrant.*

*The following nominal supply voltages are recommended: 1.0, 1.5, 3, 4, 5, 6, 9, 12, 15, 24, 30, 60, 75, 100, 150, 200 volts. These are to be published in IEC (147) Publications.*

#### 5.1.2 Additional Conditions for Static Tests

##### \* 5.1.2.1 Operating Temperature(s)

The static characteristics are registered as 25°C  $T_{A(ambient)}$   
 $T_{C(case)}$

##### 5.1.2.2 Operating Temperature Extremes, $T_{A(ambient)}$ or $T_{C(case)}$

(Min) \_\_\_\_\_°C (Max) \_\_\_\_\_°C

*If operating temperature extremes are listed, the static characteristics must also be registered at these temperature extremes. The following temperatures are recommended for operating temperature extremes: -55°C, -25°C, -10°C, 0°C, +55°C, +75°C, +100°C, +125°C.*

*The same temperature reference (ambient or case) should be used as specified in 5.1.2.1.*

##### \* 5.1.2.3 Method of Test

*State the method of test.*

*One of the following is required.*

1. DC Stabilized    *The time of application of bias conditions should be sufficient to assure a stable device temperature.*

*or*

2. Pulsed - The time duration of the test in the pulsed cycle \_\_\_\_\_s.

The time to the next test in the pulsed cycle \_\_\_\_\_s.

*The time of application of bias conditions should be so short as to cause relatively little increase in device temperature.*

## 5.2 Static Characteristics

Test conditions and limits for registration purposes must be presented for the worst case input, output loading at 25°C and at the temperature extremes of 5.1.2.2, if an operating range is claimed.

See Microelectronics Engineering Bulletin No. 5A, "Methods of Measurement for Semiconductor Logic Gating Microcircuits," which describes and defines the symbols and tests required and recommended by the following paragraphs.

The following required tests apply directly to simple inverting logic gates. One of the sequences of tests listed under Sections 5.2.1, 4.2.2 and 5.2.3, where applicable to the type circuit configuration used, should be chosen and the required registration data provided. For multiple duplicate gates these tests apply for each gate. For more complex combinations of gates, these tests should serve as guiding rules in specifying the circuits. Conditions on all terminals must be specified for each test.

### 5.2.1 Characteristics for Logic Gating Circuit (for circuits such as DCTC, RTL, and RCTL NOR Logic Gates).

#### Conditions and Tests

	<u>Values</u>	<u>Units</u>
<u>Operating Temperatures</u>	-----	°C
* 5.2.1.1 A: $V_{IL\min}$	-----	V
B: $V_{IL\max}$	-----	V
* 5.2.1.2 A: $V_{IH\min}$	-----	V
B: $V_{IH\max}$	-----	V
* 5.2.1.3 $V_{OH\min}$ with $V_I = V_{IL\max}$ applied to all inputs simultaneously, measured at $I_O \leq 0$ , where $V_{OH\min} \geq V_{IH\min}$	-----	V
* 5.2.1.4 $V_{OL\max}$ with $V_I = V_{IH\min}$ applied to each input sequentially, other inputs to $V_I = V_{IL\min}$ , measured at $I_O \geq 0$ , where $V_{OL\max} \leq V_{IL\max}$	-----	A



	<u>Values</u>	<u>Units</u>
* 5.2.1.5 A: $I_{IH}^{max}$	-----	A
with $V_I \geq V_{IH}^{min}$ applied to each input sequentially, other inputs to $V_I = V_{IL}^{min}$ , measured at $I_0 = 0$ .	-----	V
B: $I_{IH}^{max}$	-----	A
with $V_I \geq V_{IH}^{min}$ applied to each input sequentially, other inputs to $V_I \geq V_{IH}^{min}$ , measured at $I_0 = 0$ .	-----	V
5.2.1.6 $I_{OH}^{max}$	-----	A
with $V_I = V_{IL}^{max}$ applied to all inputs simultaneously, $V_{CC}$ termin- al open, measured at $V_0$ , where $V_0 \geq V_{IH}^{min}$ .	-----	V
5.2.1.7 A: $V_{OL}^{max}$	-----	V
with $V_I = V_{IH}^{max}$ applied to each input sequentially, other inputs to $V_I = V_{IL}^{min}$ , measured at $I_0 \geq 0$ , where $V_{OL}^{max} \leq V_{IL}^{max}$ .	-----	A
B: $V_{OL}^{max}$	-----	V
with $V_I = V_{IH}^{max}$ applied to all inputs simultaneously, measured at $I_0 \geq 0$ , where $V_{OL}^{max} \leq V_{IL}^{max}$ .	-----	A
5.2.1.8 $I_{OH}^{max}$	-----	A
with $V_I = V_{IL}^{min}$ applied to all inputs simultaneously, measured at $V_0$ , where $V_0 \leq V_{IH}^{max}$ .	-----	V
5.2.1.9 $I_{IH}^{max}$	-----	A
with $V_I \leq V_{IH}^{max}$ applied to each input sequentially, other inputs to $V_I = V_{IL}^{min}$ , measured at $I_0 \geq 0$ .	-----	A

	<u>Values</u>	<u>Units</u>
5.2.1.10 $I_{Omax}$ with $V_I = V_{ILmin}$ applied to all inputs simultaneously, measured at $V_O = 0$ volts.	-----	A
5.2.1.11 $V_{Omax}$ with $V_I = V_{IHmin}$ applied to each input sequentially, other inputs to $V_I = V_{ILmin}$ , $V_{CC}$ terminal open, measured at $I_O \geq 0$ .	-----	V
	-----	A

5.2.2 Characteristics for Logic Gating Circuit (*for circuits such as DTL and TTL NAND Logic Gates*).

Conditions and Tests

	<u>Values</u>	<u>Units</u>
<u>Operating Temperatures</u>		
	25	°C
* 5.2.1.1 A: $V_{ILmin}$	-----	V
B: $V_{ILmax}$	-----	V
* 5.2.1.2 A: $V_{IHmin}$	-----	V
B: $V_{IHmax}$	-----	V
* 5.2.2.3 $V_{OLmax}$ with $V_I = V_{IHmin}$ applied to all inputs simultaneously, measured at $I_O \geq 0$ , where $V_{OLmax} \leq V_{ILmax}$ .	-----	V
	-----	A
* 5.2.2.4 $I_{ILmax}$ with $V_I \leq V_{ILmax}$ applied to each input sequentially, other inputs to $V_I = V_{IHmax}$ .	-----	A
	-----	V

	<u>Values</u>	<u>Units</u>
* 5.2.2.5 A: $I_{IH}^{max}$	-----	A
with $V_I \geq V_{IH}^{min}$ applied to		
each input sequentially,	-----	V
other inputs to $V_{IL}^{min}$ ,		
measured at $I_0 = 0$ .		
(and)		
B: $I_{IH}^{max}$	-----	A
with $V_I \geq V_{IH}^{min}$ applied to		
each input sequentially,	-----	V
other inputs open or to		
$V_I \geq V_{IH}^{min}$ , measured at $I_0 = 0$ .		
* 5.2.2.6 High Level Output with $V_I = V_{IL}^{max}$		
applied to each input sequentially,		
other inputs to $V_I \geq V_{IH}^{min}$ .	-----	V
(One of the following is required)		
a) $I_{OH}^{max}$ (for outputs with no	-----	A
current source)		
measured at $V_0 \geq V_{IH}^{min}$	-----	V
(or)		
b) $V_{OH}^{min}$ (for outputs with no	-----	V
current source)		
measured for $I_0 \leq 0$ ,	-----	A
where $V_{OH}^{min} \geq V_{IH}^{min}$ .		
* 5.2.2.7 $I_0^{max}$ and/or $I_0^{min}$	-----	A
with $V_I = V_{IL}^{min}$ applied to	-----	A
all inputs simultaneously,		
measured at $V_0 \leq V_{IL}^{max}$ .	-----	V
(Required only when output has		
"pull-up" capabilities.)		
5.2.2.8 $I_{INL}^{max}$ (on input node terminals,	-----	A
if available)		
measured at $V_{INL}$ .	-----	V

	<u>Values</u>	<u>Units</u>
5.2.2.9 High Level Output with $V_{INH}$ applied to node input, other inputs open or to $V_I \geq V_{IHmin}$ .	-----	V
	-----	V
(One of the following is appropriate)		
a) $I_{OHmax}$ (for outputs with no current source)	-----	A
measured at $V_O \geq V_{IHmin}$	-----	V
(or)		
b) $V_{OHmin}$ (for outputs with current source)	-----	V
measured at $I_O \geq 0$ ,	-----	A
where $V_{OHmin} \leq V_{IHmin}$ .		
5.2.2.10 $I_{Rmax}$ and/or $I_{Rmin}$	-----	A
(for "pull-up" collector resistors where applicable and not connected to the output terminal)		
measured at $V_R \leq V_{ILmax}$ .	-----	V
5.2.3 Characteristics for Logic Gating Circuit (for circuits such as ECL with NOR and OR Logic).		
* 5.2.3.1 A: $V_{IHmin}$	-----	V
B: $V_{IHmax}$	-----	V
* 5.2.3.2 A: $V_{ILmin}$	-----	V
B: $V_{ILmax}$	-----	V
* 5.2.3.3 Reference Voltage (If an external voltage is necessary, one of the following is required.)		
a) $V_{BB}$	-----	V
Tolerance on $V_{BB}$	-----	V
(or)		
b) $V_{BB}$ specified for each temperature	-----	V
Tolerance on $V_{BB}$	-----	V

EIA TYPE NO.

	<u>Values</u>	<u>Units</u>
* 5.2.3.4 $I_{OH\min}$ (minimum fan-out current)	-----	A
* 5.2.3.5 Output Load If there is no internal load resistor, specify $I_0$ as required.	-----	A
If there is an internal load resistor, specify $I_0 = 0$ .		
5.2.3.6 $\Delta V_{OH\max}$ (change in high output voltage from $I_0 = I_{OH\min}$ to $I_0 = 0$ )	-----	V
* 5.2.3.7 $V_{OH\max}$ for NOR outputs, with $V_I = V_{IL\min}$ applied to all inputs simultaneously, measured at $I_0$ (see 5.2.3.5).	-----	V
where $V_{OH\max} \leq V_{IH\max}$ .		A
* 5.2.3.8 $V_{OH\min}$ for NOR outputs, with $V_I = V_{IL\max}$ applied to all inputs simultaneously, measured at $I_0 = I_{OH\min}$ , where $V_{OH\min} \geq V_{IH\min}$ .	-----	V
* 5.2.3.9 $V_{OL\max}$ for NOR outputs, with $V_I = V_{IH\min}$ applied to each input sequentially, other inputs to $V_I = V_{IL\min}$ , measured at $I_0$ (see 5.2.3.5),	-----	V
where $V_{OL\max} \leq V_{IL\max}$ .		A
5.2.3.10 $V_{OL\max}$ for NOR inputs with $V_I = V_{IH\max}$ applied to all inputs simultaneously, measured at $I_0$ (see 5.2.3.5),	-----	V
where $V_{OL\max} \leq V_{IL\max}$		A
* 5.2.3.11 $V_{OL\min}$ for NOR outputs with $V_I = V_{IH\max}$ applied to all inputs simultaneously, measured at $I_0$ (see 5.2.3.5)	-----	V
where $V_{OL\min} \geq V_{IL\min}$ .		A

	<u>Values</u>	<u>Units</u>
* 5.2.3.12 $V_{OL\min}$ for OR outputs with $V_{IL} = V_{IL\max}$ applied to all inputs simultaneously, measured at $I_0$ (see 5.2.3.5), where $V_{OL\min} \leq V_{IL\min}$ .	-----	V
	-----	A
* 5.2.3.13 $V_{OL\max}$ for OR outputs with $V_I = V_{IL\max}$ applied to all inputs simultaneously, measured at $I_0$ (see 5.2.3.5), where $V_{OL\max} \leq V_{IL\max}$ .	-----	V
	-----	A
* 5.2.3.14 $V_{OH\min}$ for OR outputs with $V_I = V_{IH\min}$ applied to each input sequentially, other inputs to $V_I = V_{IL\min}$ , measured at $I_0 = I_{OH\min}$ , where $V_{OH\min} \geq V_{IH\min}$ .	-----	V
* 5.2.3.15 $V_{OH\max}$ for OR outputs with $V_I = V_{IH\max}$ applied to all inputs simultaneously, measured at $I_0$ (see 5.2.3.5), where $V_{OH\max} \leq V_{IH\max}$ .	-----	V
	-----	A
* 5.2.3.16 $I_{IH\max}$ with $V_I \geq V_{OH\min}$ applied to each input sequentially, other inputs at $V_I = V_{IL\min}$ .	-----	A
* 5.2.3.17 $I_{IL\max}$ with $V_I = V_{IL\min}$ applied to each input sequentially, other inputs at $V_I = V_{IH\max}$ .	-----	A
5.2.3.18 $I_{0\min}$ and/or $I_{0\max}$ for NOR outputs, with $V_I = V_{IH\max}$ applied to all inputs simultaneously, measured at $V_0 \geq V_{IH\min}$ .	-----	A
	-----	V
5.2.3.19 $I_{0\min}$ and/or $I_{0\max}$ for OR outputs, with $V_I = V_{IL\min}$ applied to all inputs simultaneously, measured at $V_0 \geq V_{IH\min}$ .	-----	A
	-----	V

### 5.3 Dynamic Characteristics, 25°C

In all tests except where otherwise noted, the nominal value of all supply voltages ( $V_{CC}$ ,  $V_{EE}$ ,  $V_{BB}$ , etc.) is applied (see Item 5.1.1).

*See Microelectronics Engineering Bulletin No. 5A, "Methods of Measurement for Semiconductor Logic Gating Microcircuits," which describes and defines the symbols and the tests required and recommended by the following paragraphs.*

#### 5.3.1 Propagation Delay Time

	<u>Min</u>	<u>Max</u>
* 5.3.1.1 $t_{PLH}$	_____	_____s
* 5.3.1.2 $t_{PHL}$	_____	_____s

*(These times should apply to all input-output relations that have the same logic equations as called out in Section 2.2. If several different basic logical information paths exist, different times shall be specified for each equation, if the above do not apply.)*

#### \* 5.3.1.3 Conditions for Propagation Delay Time Measurement

*When applicable, tolerances should be applied to the input pulse parameters requested.*

a. Pulse generator impedance	_____ $\Omega$
b. Input waveform at [pulse generator, driver or input to C.U.T. <sup>(1)</sup> ]	
$t_{TLH}$	_____s
$t_{THL}$	_____s
amplitude LOW	_____V
HIGH	_____V
width of ( <u>HIGH or LOW</u> ) pulse	_____s
repetition rate	_____Hz
c. $C_I$ (if not included in driving network)	_____F
$C_O$ (if not included in loading network)	_____F

<sup>(1)</sup> Symbols are defined the same as for output waveforms.

EIA TYPE NO.

d. Bias on unused inputs of C.U.T. \_\_\_\_\_ V

Bias and/or loading on unused outputs of C.U.T. \_\_\_\_\_ V

Show schematic if appropriate. Figure No. \_\_\_\_\_

e. Oscilloscope probe impedance \_\_\_\_\_  $\Omega$

f. 1. Type of driving circuit \_\_\_\_\_

Use registered number where possible.

Type of loading circuit \_\_\_\_\_

Use registered number where possible.

Multiplicity of driving (M) and loading (N) circuits: \_\_\_\_\_

	<u>Max</u>		<u>Max</u>	
	M	N	M	N
$t_{PLH}$	_____	_____	_____	_____
$t_{PHL}$	_____	_____	_____	_____

Bias on unused inputs and outputs of driving and loading circuits Figure No. \_\_\_\_\_

Show by logic diagram.

OR

Note that driver and load need not be both circuits nor both networks.

2. Schematic of driving network Figure No. \_\_\_\_\_

(If several are used indicate for which each measurement is appropriate.)

Schematic of output loading network Figure No. \_\_\_\_\_

(If several are used indicate for which measurement each is appropriate.)

### 5.3.2 Output Transition Times

	<u>Min</u>	<u>Max</u>
* 5.3.2.1 $t_{THL}$	_____	_____ s
* 5.3.2.2 $t_{TLH}$	_____	_____ s

(These times should apply to all input-output relations that have the same logic equations as called out in Section 2.2. If several different basic logical information paths exist, different times shall be specified for each equation, if the above do not apply.)



\* 5.3.2.3 Conditions for Output Transition Time Measurements

Where applicable, tolerances should be applied to the input pulse parameters requested.

- a. Pulse generator impedance \_\_\_\_\_  $\Omega$
- b. Input waveform at [pulse generator, driver  
or input to C.U.T. (1)]
  - $t_{TLH}$  \_\_\_\_\_ s
  - $t_{THL}$  \_\_\_\_\_ s
  - amplitude LOW \_\_\_\_\_ V
  - HIGH \_\_\_\_\_ V
  - width of (HIGH or LOW) pulse \_\_\_\_\_ s
  - repetition rate \_\_\_\_\_ Hz
- c.  $C_I$  (if not included in driving network) \_\_\_\_\_ F
- $C_O$  (if not included in loading network) \_\_\_\_\_ F
- d. Bias on unused inputs of C.U.T. \_\_\_\_\_ V
- Bias and/or loading on unused outputs of C.U.T. \_\_\_\_\_ V
- Show schematic if appropriate. Figure No. \_\_\_\_\_
- e. Oscilloscope probe impedance \_\_\_\_\_  $\Omega$
- f. Voltage level for HIGH state  $t_{THL}$   $t_{TLH}$   
\_\_\_\_\_ V \_\_\_\_\_ V
- Voltage level for LOW state \_\_\_\_\_ V \_\_\_\_\_ V
- g. 1. Type of driving circuit \_\_\_\_\_  
Use registered number where possible.  
Bias on unused inputs and outputs  
of driving circuit Figure No. \_\_\_\_\_  
Show by logic diagram.  
OR
2. Schematic of driving network Figure No. \_\_\_\_\_  
(If several are used indicate for  
which each measurement is appropriate.)
- h. Schematic of loading network Figure No. \_\_\_\_\_  
(If several are used indicate for  
which each measurement is appropriate.)

(1) Symbols are defined the same as for output waveforms.

\* 5.4 Power Supply Current Drain at +25°C  $T_{A(ambient)}$  or  $T_{C(case)}$  temperature.

*The same temperature reference (ambient or case) should be used as specified in 5.1.2.1.*

With the nominal power supply voltage and all output terminals open-circuited. (See Item 5.1.1.)

*Two input logic conditions shall be specified. The first condition shall have the maximum sum of the absolute magnitude of all power supply currents. For these two conditions the maximum supply current shall be specified for each power supply. A description of the test circuit shall be provided.*

5.4.1 Maximum Current Drain Condition

- |         |                             |                   |                 |
|---------|-----------------------------|-------------------|-----------------|
| 5.4.1.1 | $V_{CC}$                    | (____volts) Drain | ____A           |
| 5.4.1.2 | $V_{EE}$                    | (____volts) Drain | ____A           |
| 5.4.1.3 | $V_{BB}$                    | (____volts) Drain | ____A           |
| 5.4.1.4 | $V_{other}$                 | (____volts) Drain | ____A           |
| 5.4.1.5 | Description of Test Circuit |                   | Figure No. ____ |

5.4.2 Minimum Current Drain Condition

- |         |                             |                   |                 |
|---------|-----------------------------|-------------------|-----------------|
| 5.4.2.1 | $V_{CC}$                    | (____volts) Drain | ____A           |
| 5.4.2.2 | $V_{EE}$                    | (____volts) Drain | ____A           |
| 5.4.2.3 | $V_{BB}$                    | (____volts) Drain | ____A           |
| 5.4.2.4 | $V_{other}$                 | (____volts) Drain | ____A           |
| 5.4.2.5 | Description of Test Circuit |                   | Figure No. ____ |

INSTRUCTIONS FOR USE OF THE DATA FORMAT

1. *The minimum specifications are covered by asterisked items. An asterisked item may be omitted only when sound technical justifications are supplied.*
2. *Additional data which further characterize the device may be supplied. These data may consist of additional ratings or characteristics or a repetition of data under other operating or terminal conditions.*
3. *The data supplied should adequately define the device in terms of interchangeability in the intended application and should distinguish it from existing registered devices.*
4. *When preparing a registration data sheet for release, delete italicized notes, all unused items, and all asterisks. Where necessary, renumber the items in proper sequence.*
5. *Existing EIA and JEDEC standards for measurement methods, preferred values, definitions, and letter symbols shall be used as applicable. MED Bulletin No. 5A is intended as a guide to this format.*

## APPENDIX I

### 1.0 CONDITIONS FOR APPLICABILITY OF FORMAT

- 1.1 This format is intended to register the lowest level unit assembly.
- 1.2 The part is tested and intended for use as a logic gating circuit, multiple logic gating circuit, or a complex combination of logic gating circuits.
- 1.3 The part is a microcircuit as defined by the Microelectronics Engineering Bulletin 1A. Included within the definition of Microcircuits are Multichip Microcircuits, Hybrid Microcircuits, Monolithic Integrated Circuits, and Film Integrated Circuits.

### 2.0 DEFINITIONS OF SEMICONDUCTOR LOGIC GATING MICROCIRCUITS

- 2.1 Monolithic - elements formed in situ on or within a semiconductor substrate with at least one of the elements formed within the substrate.
- 2.2 Multichip - elements formed on or within two or more semiconductor chips which are separately attached to a substrate.
- 2.3 Film - elements are films formed in situ on an insulating substrate.
- 2.4 Hybrid - an integrated logic gate other than above, commonly consisting of any two or more of the following: monolithic, film, and discrete elements inseparably associated on a continuous substrate.

